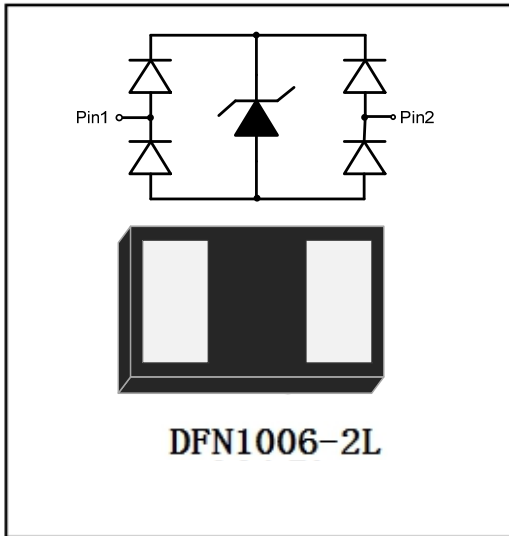


1- Line, Bi-directional, Ultra-low Capacitance Transient Voltage Suppressor



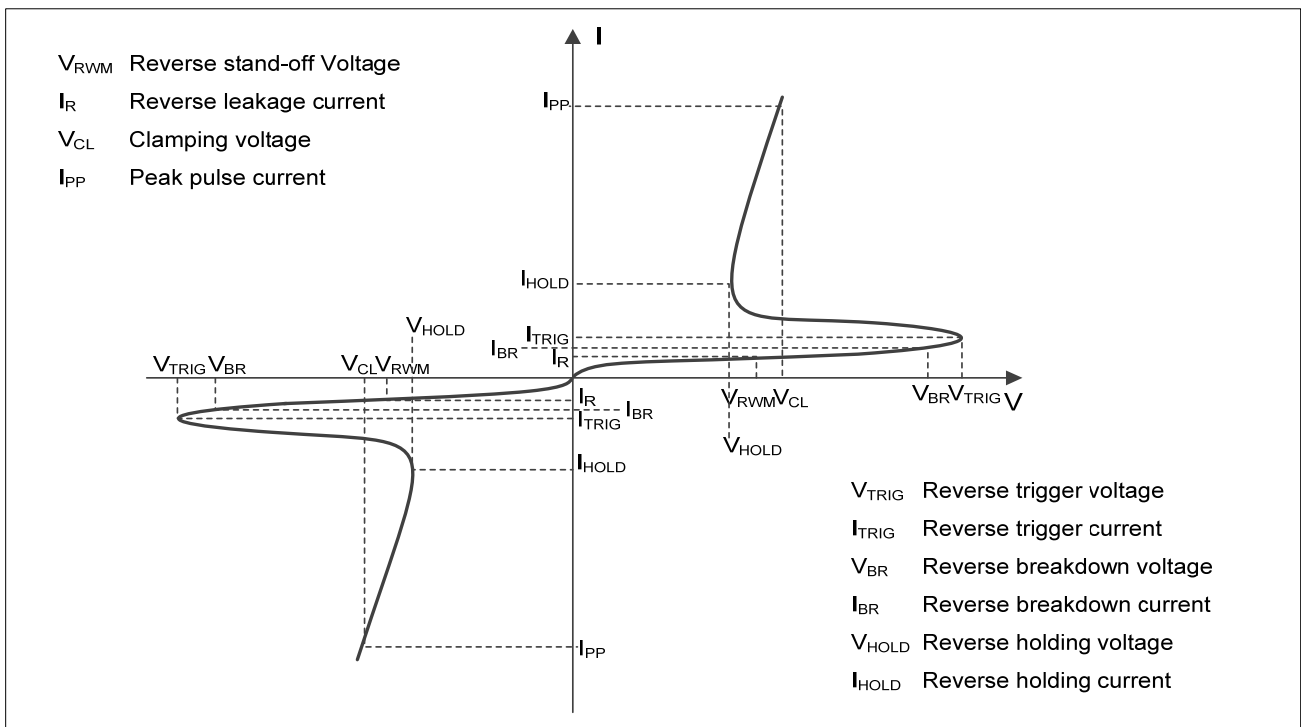
Features

- Stand-off voltage: 18V Max
- Transient protection for each line according to IEC61000-4-2(ESD): $\pm 15\text{kV}$ (contact)
IEC61000-4-5(surge): 4A (8/20 μs)
- Ultra-low capacitance: $C_J = 0.35\text{pF}$ typ
- Ultra-low leakage current: $I_R < 1\text{nA}$ typ.
- Low clamping voltage: $V_{CL} = 10\text{V}$ typ. @ $I_{PP} = 16\text{A}$ (TLP)
- Solid-state silicon technology

Mechanical Data

- **Package:** DFN1006-2L
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Polarity:** Cathode line denotes the cathode end
- **Marking:** 8U

■Definitions of Electrical Characteristics





ESDSL18VLB

■Maximum Ratings

| PARAMETER | SYMBOL | Rating | UNIT |
|---|-----------|----------|-------------|
| Peak pulse power ($t_p = 8/20\mu s$) | P_{pk} | 40 | W |
| Peak pulse current ($t_p = 8/20\mu s$) | I_{PP} | 4 | A |
| ESD according to IEC61000-4-2 air discharge | V_{ESD} | ± 15 | KV |
| ESD according to IEC61000-4-2 contact discharge | | ± 15 | KV |
| Junction temperature | T_J | 125 | $^{\circ}C$ |
| Operating temperature | T_{OP} | -40~85 | $^{\circ}C$ |
| Storage temperature | T_{STG} | -55~150 | $^{\circ}C$ |

■Electrical Characteristics ($T_a=25^{\circ}C$ Unless otherwise specified)

| PARAMETER | Symbol | UNIT | Conditions | Min | Typ | Max |
|----------------------------------|-----------|----------|--------------------------------|------|------|----------|
| Reverse maximum working voltage | V_{RWM} | V | | | | ± 18 |
| Reverse leakage current | I_R | nA | $V_{RWM} = 18V$ | | <1 | 50 |
| Reverse breakdown voltage | V_{BR} | V | $I_{BR} = 1mA$ | 18.5 | | |
| Clamping voltage ¹⁾ | V_{CL} | V | $I_{PP} = 16A, t_p = 100ns$ | | 10.0 | |
| Dynamic resistance ¹⁾ | R_{DYN} | Ω | | | 0.25 | |
| Clamping voltage ²⁾ | V_{CL} | V | $V_{ESD} = 8kV$ | | 10.0 | |
| Clamping voltage ³⁾ | V_{CL} | V | $I_{PP} = 1A, t_p = 8/20\mu s$ | | 5 | 6 |
| | | V | $I_{PP} = 4A, t_p = 8/20\mu s$ | | 9 | 10 |
| Junction capacitance | C_J | pF | $V_R = 0V, f = 1MHz$ | | 0.35 | 0.5 |

(1). TLP parameter: $Z_0 = 50\Omega, t_p = 100ns, t_r = 2ns$, averaging window from 60ns to 80ns. R_{DYN} is calculated from 4A to 16A.

(2). Contact discharge mode, according to IEC61000-4-2.

(3). Non-repetitive current pulse, according to IEC61000-4-5.

■Ordering Information (Example)

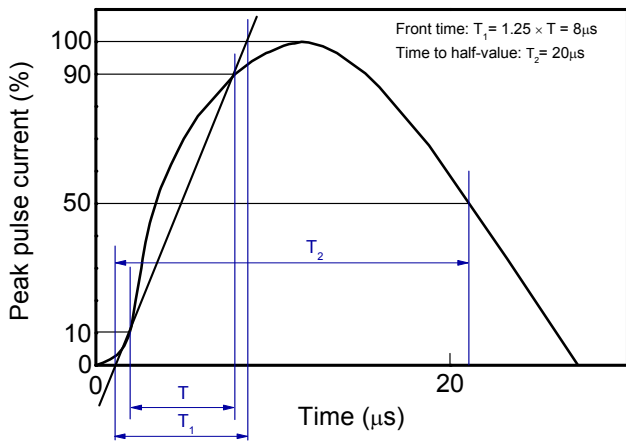
| PREFERRED P/N | UNIT WEIGHT(mg) | MINIMUM PACKAGE(pcs) | INNER BOX QUANTITY(pcs) | OUTER CARTON QUANTITY(pcs) | DELIVERY MODE |
|---------------|-----------------|----------------------|-------------------------|----------------------------|---------------|
| ESDSL18VLB | Approximate 0.9 | 10000 | 100000 | 400000 | Tape&reel |



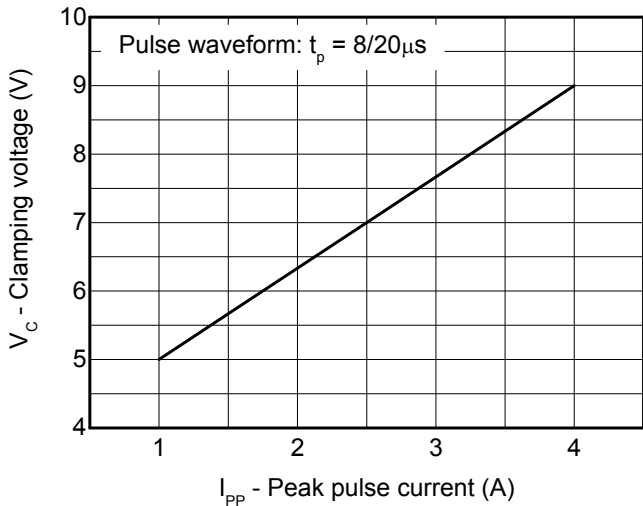
ESDLC18VLB

■ Characteristics (Typical)

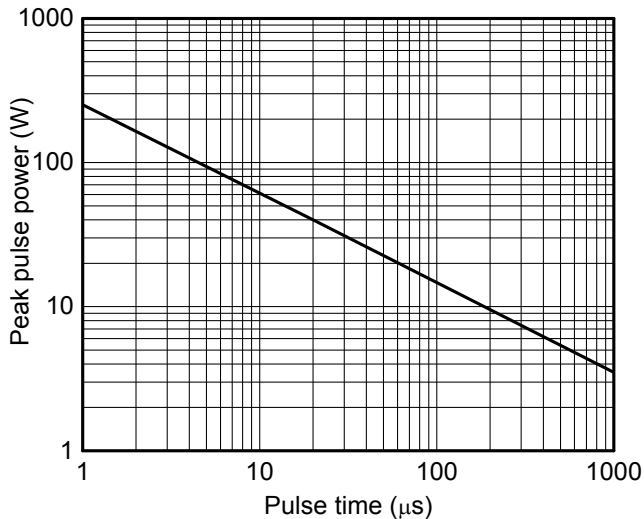
8/20 μ s waveform per IEC61000-4-5



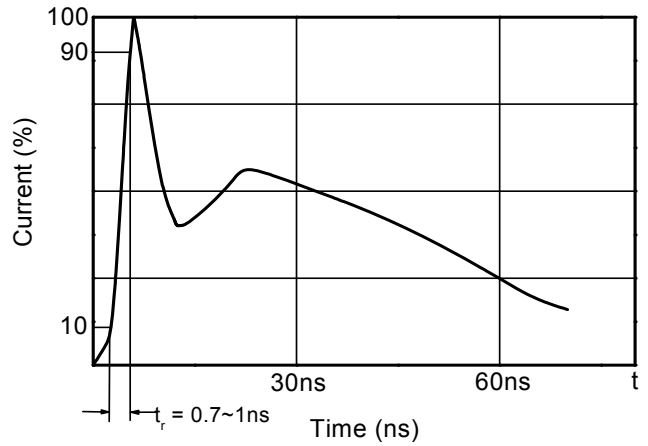
Clamping voltage vs. Peak pulse current



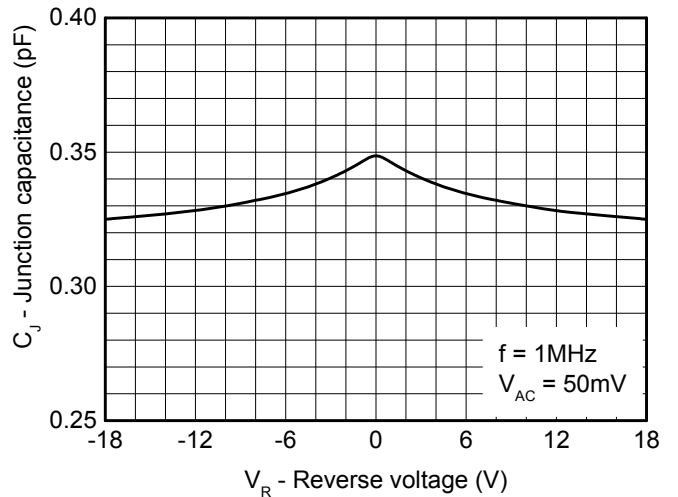
Non-repetitive peak pulse power vs. Pulse time



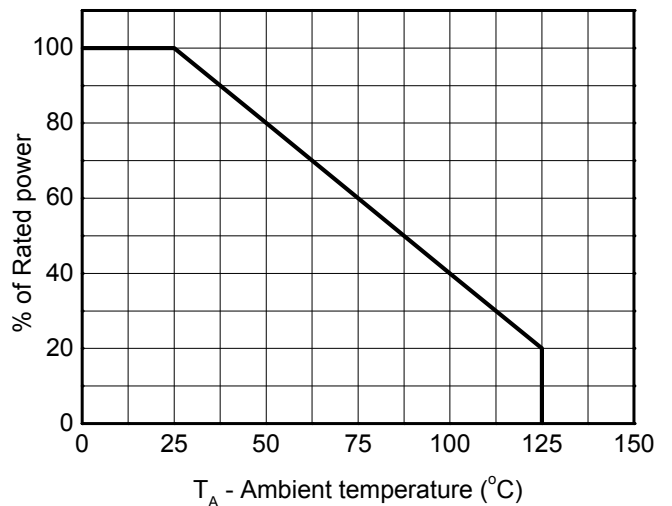
Contact discharge current waveform per IEC61000-4-2



Capacitance vs. Reverse voltage



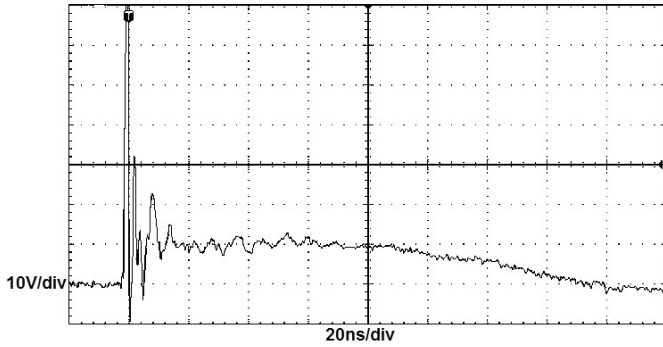
Power derating vs. Ambient temperature



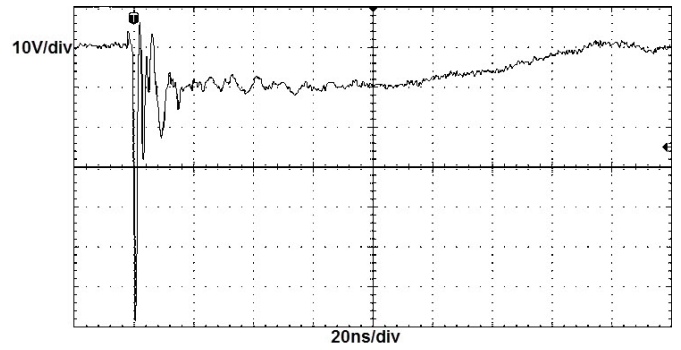


ESDSL18VLB

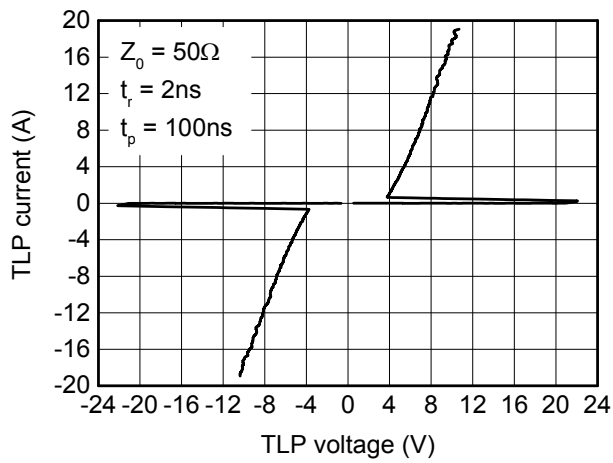
ESD clamping
(+8kV contact discharge per IEC61000-4-2)



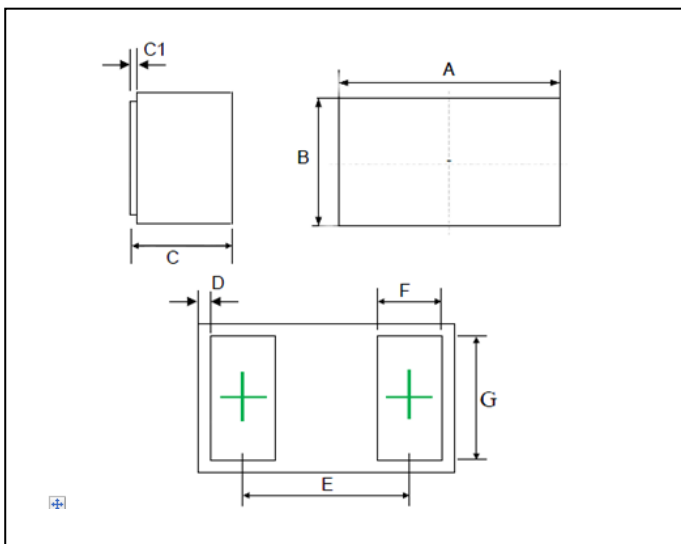
ESD clamping
(-8kV contact discharge per IEC61000-4-2)



TLP Measurement



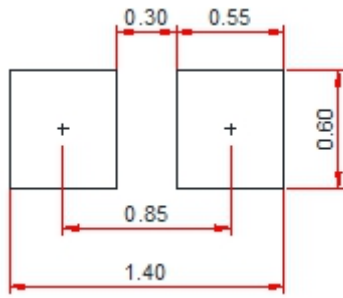
■ Outline Dimensions



| Symbol | min. (mm) | Max. (mm) |
|--------|-----------|-----------|
| A | 0.95 | 1.05 |
| B | 0.55 | 0.65 |
| C | 0.4 | 0.5 |
| C1 | | 0.05 |
| D | 0.01 | 0.08 |
| E | | 0.65 |
| F | 0.2 | 0.3 |
| G | 0.45 | 0.55 |



■ Recommend land pattern (Unit:mm)



Notes:

This recommended land pattern is for reference purposes only. Please consult your manufacturing group to ensure your PCB design guidelines are met



ESDSL18VLB

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