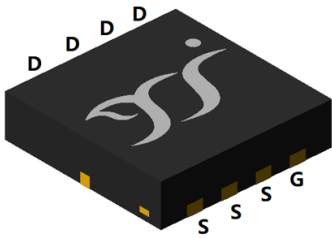
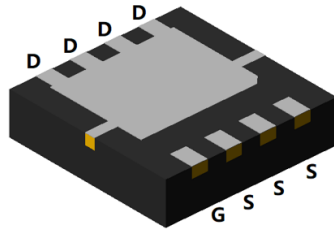


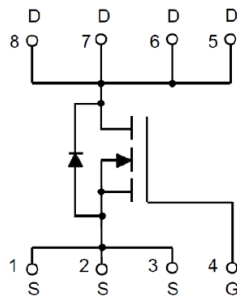
N-Channel Enhancement Mode Field Effect Transistor



Top View



Bottom View



DFN3333-8L

Product Summary

- V_{DS} 30V
- I_D 30A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) < 9 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) < 13 mohm
- 100% EAS Tested

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 3
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ C$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	30	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_A=25^\circ C$	I_D	14	A
	$T_A=100^\circ C$		9	
	$T_C=25^\circ C$		30	
	$T_C=100^\circ C$		19	
Pulsed Drain Current ^A		I_{DM}	115	A
Total Power Dissipation	$T_A=25^\circ C$	P_D	2.5	W
	$T_A=100^\circ C$		1	
	$T_C=25^\circ C$		17	
	$T_C=100^\circ C$		7	
Single Pulse Avalanche Energy ^B		E_{AS}	60.5	mJ
Thermal Resistance Junction-to-Case ^C		$R_{\theta JC}$	7.1	$^\circ C/W$
Thermal Resistance Junction-to-Ambient ^C		$R_{\theta JA}$	50	$^\circ C/W$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ C$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ30N03A	F1	Q30N03	5000	10000	100000	13" reel



YJQ30N03A

RECOMMEND
YJQ35N03A
FOR NEW DESIGN

■ Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V	T _J =25°C		1	μA
			T _J =150°C		100	
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = 10V, I _D =15A		5.8	9	mΩ
		V _{GS} = 4.5V, I _D =15A		10	13	
Diode Forward Voltage	V _{SD}	I _S =15A, V _{GS} =0V		0.85	1.2	V
Maximum Body-Diode Continuous Current	I _S				30	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHz		1015		pF
Output Capacitance	C _{oss}			201		
Reverse Transfer Capacitance	C _{rss}			164		
Gate Resistance	R _g	f=1MHz		1.5		Ω
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =20A		23.6		nC
Total Gate Charge	Q _{g(4.5V)}			12.9		
Gate-Source Charge	Q _{gs}			3.9		
Gate-Drain Charge	Q _{gd}			7		
Reverse Recovery Charge	Q _{rr}	I _F =15A, di/dt=100A/us		0.2		ns
Reverse Recovery Time	t _{rr}			5		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _{GEN} =3Ω		7		ns
Turn-on Rise Time	t _r			19		
Turn-off Delay Time	t _{D(off)}			24		
Turn-off fall Time	t _f			24		

A. Pulse Test: Pulse Width ≤ 300μs, Duty cycle ≤ 2%.

B. T_J=25°C, V_{DD}=25V, V_G=10V, L=1mH, I_{AS}=11A

C. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

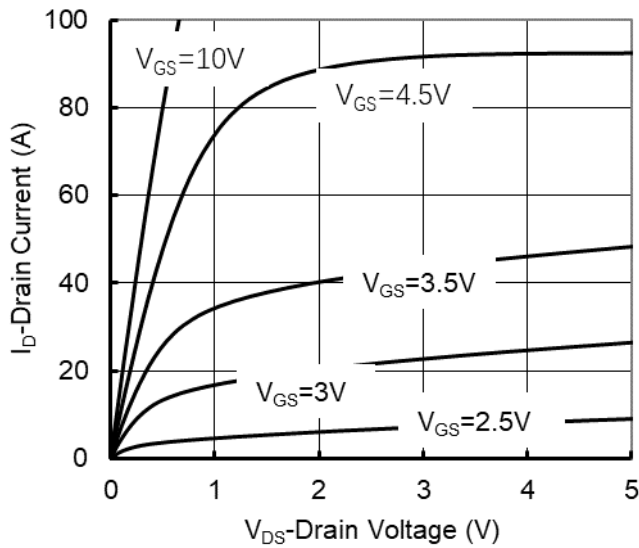


Figure1. Output Characteristics

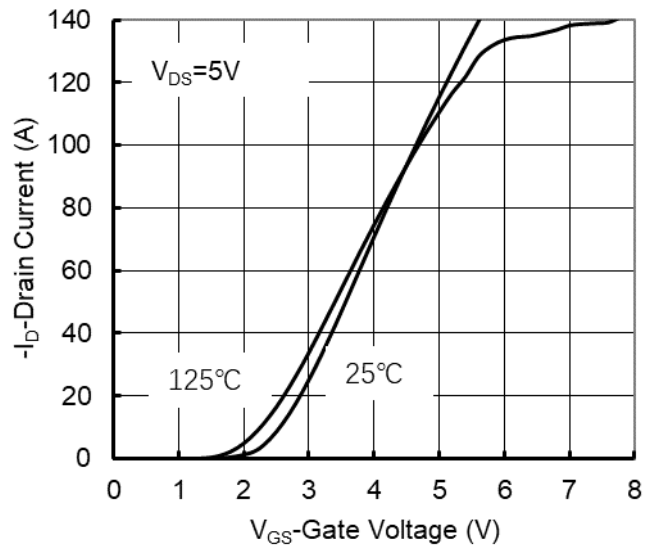


Figure2. Transfer Characteristics

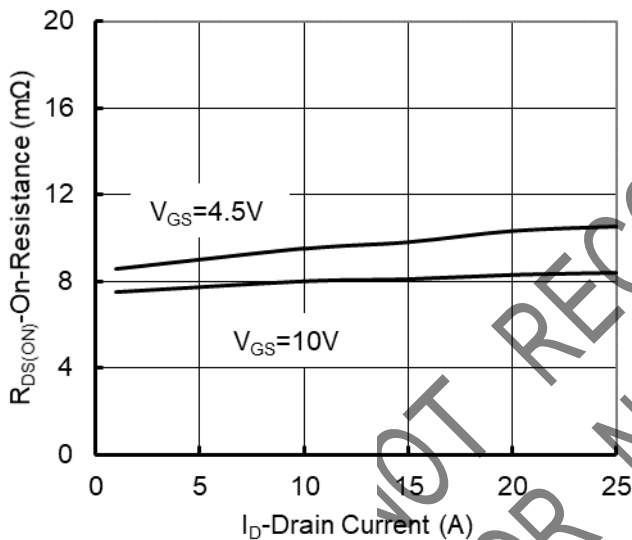


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

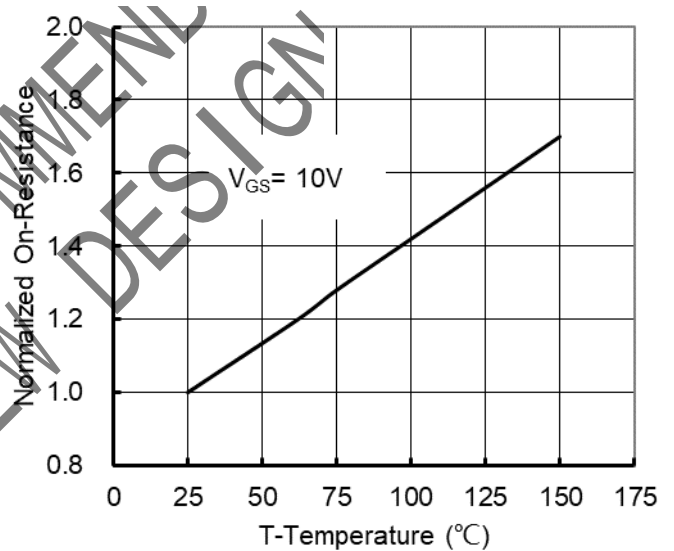


Figure 4: On-Resistance vs. Junction Temperature

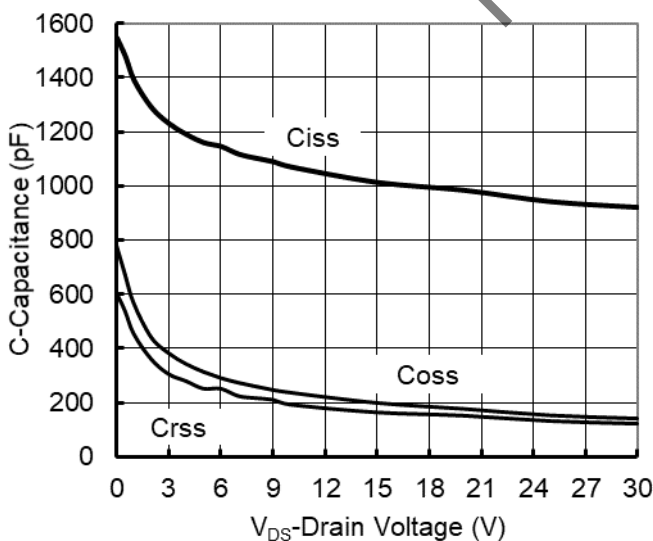


Figure5. Capacitance Characteristics

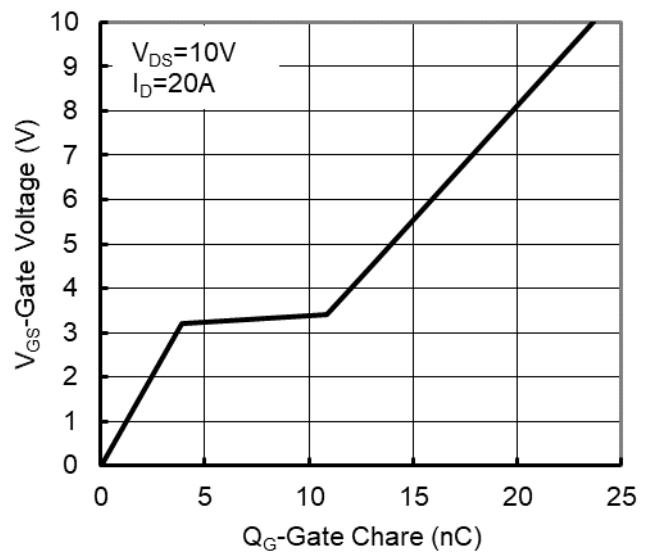


Figure6. Gate Charge

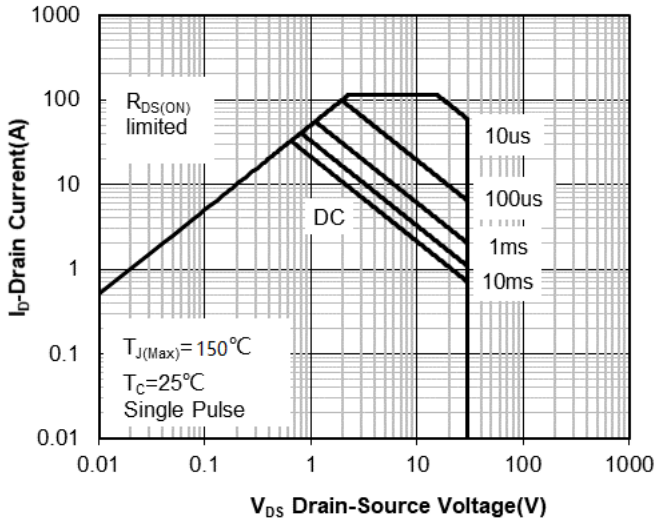


Figure7. Safe Operation Area

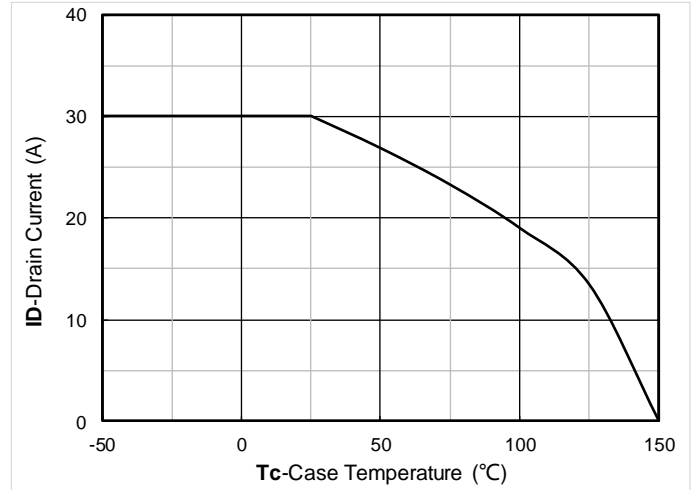


Figure8. Maximum Continuous Drain Current vs Case Temperature

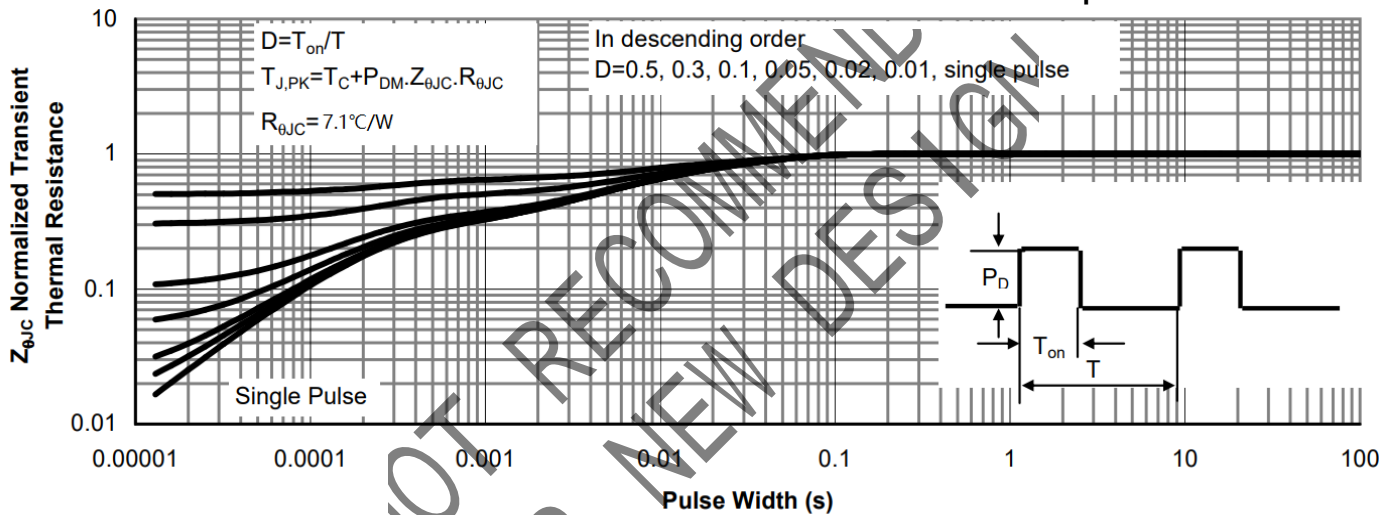
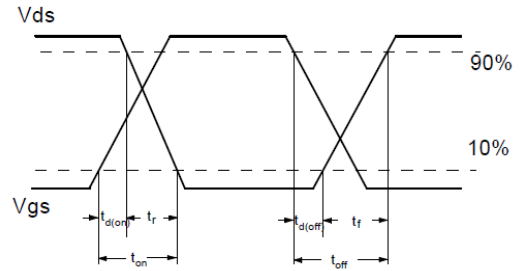
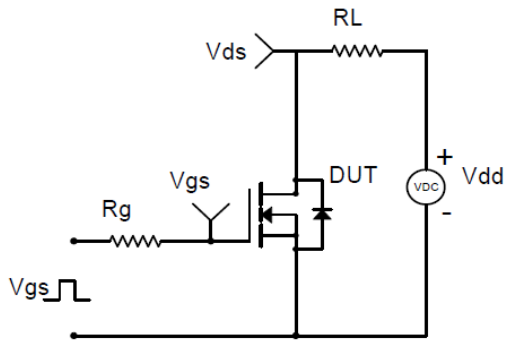
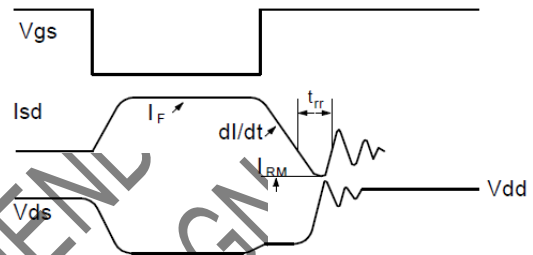
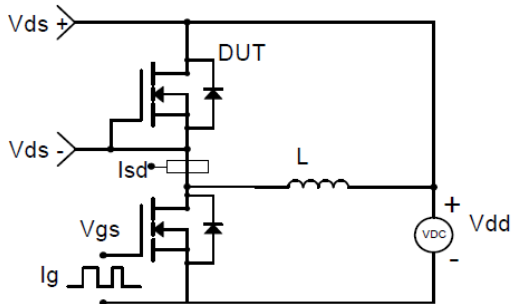


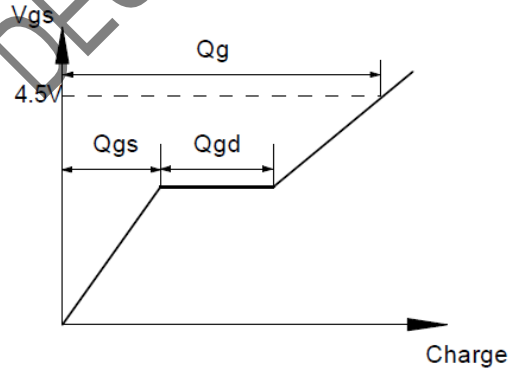
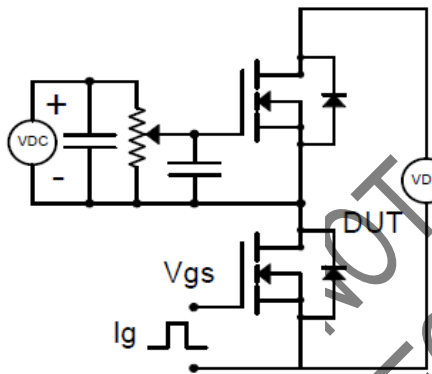
Figure9. Normalized Maximum Transient Thermal Impedance



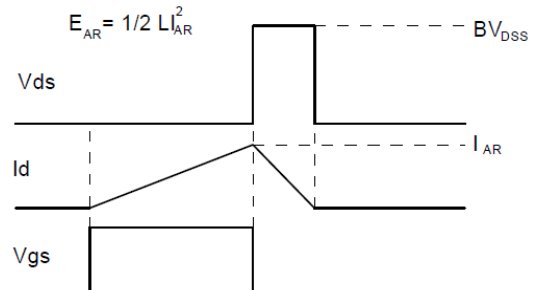
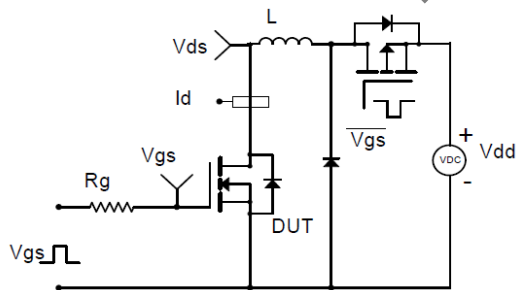
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



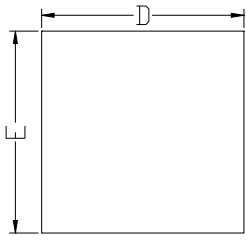
Gate Charge Test Circuit & Waveform



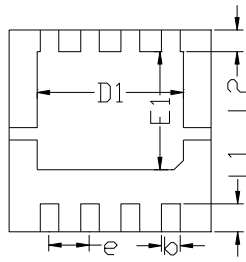
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



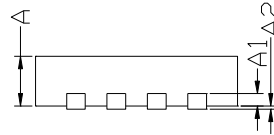
■DFN3333-8L Package information



Top View
正面视图

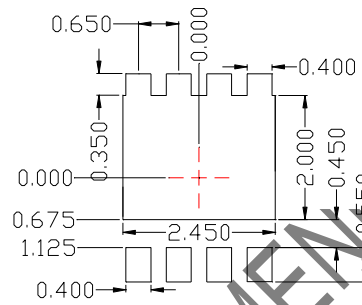


Bottom View
背面视图



Side View
侧面视图

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
D	3.15	3.25	3.35
E	3.15	3.25	3.35
A	0.70	0.80	0.90
A1	0.20 BSC		
A2			0.10
D1	2.20	2.35	2.50
E1	1.80	1.90	2.00
L1	0.35	0.45	0.55
L2	0.35 BSC		
b	0.20	0.30	0.40
e	0.65 BSC		



Suggested Solder Pad Layout
Top View

Note:

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

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